

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization International Bureau



(43) International Publication Date
24 December 2003 (24.12.2003)

PCT

(10) International Publication Number
WO 2003/107019 A3

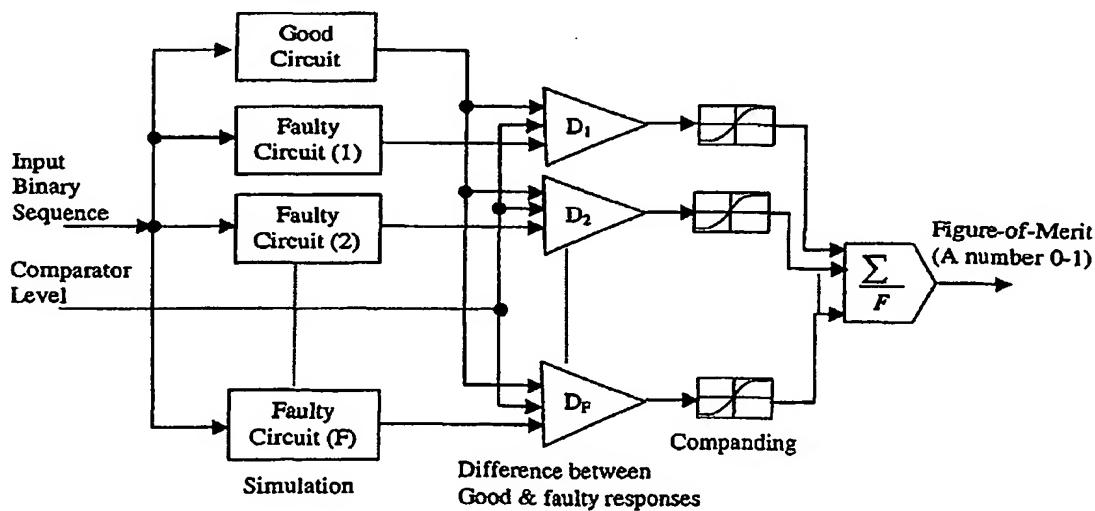
- (51) International Patent Classification⁷: **G01R 31/3167, 31/3183**
- (21) International Application Number:
PCT/GB2003/002599
- (22) International Filing Date: **17 June 2003 (17.06.2003)**
- (25) Filing Language: **English**
- (26) Publication Language: **English**
- (30) Priority Data:
0213882.4 17 June 2002 (17.06.2002) GB
- (71) Applicant (*for all designated States except US*): **UNIVERSITY OF STRATHCLYDE [GB/GB]**; McCance Building, 16 Richmond Street, Glasgow G1 1XQ (GB).
- (72) Inventors; and
- (75) Inventors/Applicants (*for US only*): **HAMILTON, David, James [GB/GB]**; 29 Belmont Gardens, Edinburgh EH12 6JD (GB). **STIMPSON, Brian, Philip [GB/GB]**; 67 Partickhill Road, Glasgow G11 5AD (GB). **BEKHEIT**,
- Mahmoud, Ali, Mousa [EG/EG]; 190A King Faisal Street, Giza, Cairo (EG).
- (74) Agents: **MacDOUGALL, Donald, Carmichael et al.**; Cruikshank & Fairweather, 19 Royal Exchange Square, Glasgow G1 3AE (GB).
- (81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.
- (84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

[Continued on next page]

(54) Title: **A DIGITAL SYSTEM AND METHOD FOR TESTING ANALOGUE AND MIXED-SIGNAL CIRCUITS OR SYSTEMS**



(57) Abstract: A method of optimising a digital test signal for testing an analogue or mixed-signal circuit comprising determining a measure, for example a figure of merit, that is indicative of differences between the output of a fault free and the output of a known faulty circuit in response to an applied digital input signal. The digital input signal is then varied and another figure of merit is calculated for the fault free and the known faulty circuit for the new input signal. This is repeated a number of times, the digital input signal being varied each time. An optimum test signal is selected based on the determined figures of merit.

WO 2003/107019 A3



- before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

- (88) Date of publication of the international search report:
1 July 2004

INTERNATIONAL SEARCH REPORT

PCT/GB 03/02599

A. CLASSIFICATION OF SUBJECT MATTER
 IPC 7 G01R31/3167 G01R31/3183

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
 IPC 7 G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC, WPI Data, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|------------|---|--------------------------|
| X | ZHENG H H ET AL: "A novel test generation approach for parametric faults in linear analog circuits" PROCEEDINGS. 14TH IEEE VLSI TEST SYMPOSIUM (CAT. NO.96TB100043), PROCEEDINGS OF 14TH VLSI TEST SYMPOSIUM, PRINCETON, NJ, USA, 28 APRIL-1 MAY 1996, pages 470-475, XP002265465 1996, Los Alamitos, CA, USA, IEEE Comput. Soc. Press, USA ISBN: 0-8186-7304-4 | 1-14, 16-34, 47-50 |
| Y | page 471, column 1, paragraph 2 -page 473, column 2, paragraph 1; figures 2-4,9 --- | 22 -/- |

Further documents are listed in the continuation of box C.

Patent family members are listed in annex.

° Special categories of cited documents :

- *A* document defining the general state of the art which is not considered to be of particular relevance
- *E* earlier document but published on or after the international filing date
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- *Y* document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
- *8* document member of the same patent family

Date of the actual completion of the international search

20 April 2004

Date of mailing of the international search report

11.05.2004

Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
 NL - 2280 HV Rijswijk
 Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
 Fax: (+31-70) 340-3016

Authorized officer

Böhm-Pélissier, A

INTERNATIONAL SEARCH REPORT

PCT/GB 03/02599

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category * | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|------------|---|------------------------------------|
| Y | SAAB D G ET AL: "CRIS: A test cultivation program for sequential VLSI circuits" PROCEEDINGS OF THE IEEE/ACM INTERNATIONAL CONFERENCE ON COMPUTER AIDEDDESIGN (ICCAD). SANTA CLARA, NOV. 8 - 12, 1992, LOS ALAMITOS, IEEE COMP. SOC. PRESS, US, vol. CONF. 10, 8 November 1992 (1992-11-08), pages 216-219, XP010094549 ISBN: 0-8186-3010-8 page 217, column 1 | 22 |
| X | VAN SPAANDONK J ET AL: "SELECTING MEASUREMENTS TO TEST THE FUNCTIONAL BEHAVIOR OF ANALOG CIRCUITS" JOURNAL OF ELECTRONIC TESTING, KLUWER ACADEMIC PUBLISHERS, DORDRECHT, NL, vol. 9, no. 1/2, 1 August 1996 (1996-08-01), pages 9-18, XP000636621 ISSN: 0923-8174 page 15 -page 16 | 1-14, 16, 20, 23, 24, 47, 48 |
| X | BALIVADA A ET AL: "A UNIFIED APPROACH FOR FAULT SIMULATION OF LINEAR MIXED-SIGNAL CIRCUITS" JOURNAL OF ELECTRONIC TESTING, KLUWER ACADEMIC PUBLISHERS, DORDRECHT, NL, vol. 9, no. 1/2, 1 August 1996 (1996-08-01), pages 29-41, XP000636623 ISSN: 0923-8174 page 33, column 2, paragraph 2 -page 35; figures 6,11; table 3 | 1, 2, 16, 20, 23, 24, 47, 48 |
| A | WO 98/55880 A (SAAB KHALED ;HAMIDA NAIM BEN (US); KAMINSKA BOZENA (US); OPMAXX IN) 10 December 1998 (1998-12-10) abstract; figures 7,8,11,13 | 1-34, 47-50 |
| X | US 5 745 409 A (SO HOCK C ET AL) 28 April 1998 (1998-04-28) abstract; figures 1,3A column 3, line 18 - line 50 column 8, line 34 -column 9, line 5 | 35-46, 51-55 |
| A | US 5 694 356 A (SO HOCK C ET AL) 2 December 1997 (1997-12-02) abstract; figure 29 | 35-46, 51-55 |
| X | US 5 748 124 A (WHYTE ROBERT ET AL) 5 May 1998 (1998-05-05) abstract; figure 1 | 35, 42, 51, 53, 55 |
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INTERNATIONAL SEARCH REPORT

PCT/GB 03/02599

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
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| A | US 5 793 778 A (QURESHI FAZAL UR REHMAN) 11 August 1998 (1998-08-11) abstract; figure 1 ----- | 35-46, 51-55 |

INTERNATIONAL SEARCH REPORT

PCT/GB 03/02599

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. Claims Nos.: because they relate to subject matter not required to be searched by this Authority, namely:

2. Claims Nos.: because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. Claims Nos.: because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see additional sheet

1. As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

- The additional search fees were accompanied by the applicant's protest.
 No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/ 210

This International Searching Authority found multiple (groups of) inventions in this international application, as follows:

1. Claims: 1-34, 47-50

These claims are related to a method/apparatus for generating digital test inputs for an analog circuit by using an optimisation algorithm.

2. Claims: 35-46, 51-55

These claims relate to a method/apparatus for testing an analog circuit by means of an optimised digital input signal for determining a fault.

INTERNATIONAL SEARCH REPORT

Information on patent family members

PCT/GB 03/02599

| Patent document cited in search report | | Publication date | | Patent family member(s) | | Publication date |
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